Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **OUTPUT 1**
2. **INPUT 1 –**
3. **INPUT 1 +**
4. **V +**
5. **INPUT 2 +**
6. **INPUT 2 -**
7. **OUTPUT 2**
8. **OUTPUT 3**
9. **INPUT 3 -**
10. **INPUT 3 +**
11. **GND**
12. **INPUT 4 +**
13. **INPUT 4 –**
14. **OUTPUT 4**

**60 mils**

**1 14**

**13**

**12**

**11**

**10**

**9**

**2**

**3**

**4**

**5**

**6**

**7 8**

**MASK**

**REF**

**55 mils**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: Floating (or GND)**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .055” X .060” DATE: 7/11/22**

**MFG: MOTOROLA THICKNESS .010” P/N: LM124**

**DG 10.1.2**

#### Rev B, 7/19/02